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Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Week 7

Week 8

Week 9

    ○ Lecture 43: SECONDARY STORAGE DEVICES

    ○ Lecture 44: INPUT-OUTPUT ORGANIZATION

Thank you for taking the Week 9 : Assignment 9.

Week 9 : Assignment 9

Your last recorded submission was on 2021-09-29, 15:30 IST   **Due date: 2021-09-29, 23:59 IST.**

1) Consider a hard disk that is rotating with a speed of 9500 rpm. The maximum rotational delay or latency will be .... milliseconds? (Give answer correct up-to two decimal places).

> 6.31

1 point

2) Which of the following memory devices cannot be used for backup (or as a secondary storage device)?

     a. DRAM
     b. SRAM
     c. Floppy Disk
     d. Hard Disk
     e. Flash Memory

1 point

☑ a.
☑ b.
☐ c.
☐ d.
☐ e.

3) Which of the following statement(s) is/are true for hard disk?

1 point

    a. It is faster than Solid-state drives.

    b. Sector is the smallest unit of data transfer.

    c. It does not have any moving parts.

    d. It is volatile in nature.

    e. None of these.

☐ a.

☑ b.

☐ c.

☐ d.

☐ e.

4) Consider a hard disk with 2 double sided platters, 2500 tracks per surface, 200 sectors per track, and sector size of 1024 bytes. The total capacity of the disk will be .... Giga bytes. (Assume 1024 = 1K)

1.90

1 point

5) Which of the following operation is used to read a bit from floating gate transistor?

1 point

    a. Apply read voltage at control gate and measure drain current.

    b. Apply read voltage at control gate and measure source current.

    c. Apply read voltage at floating gate and measure drain current.

    d. Apply read voltage at floating gate and measure source current.

◉ a.

○ b.

○ c.

○ d.

6) Which of the following statement(s) is/are true for I/O device interfacing?

     a. An input port is implemented using a tri-state bus driver.
     b. An input port is implemented using a parallel-in parallel-out register.
     c. An output port is implemented using a tri-state bus driver.
     d. An output port is implemented using a parallel-in parallel-out register.

- ☑ a.
- ☐ b.
- ☐ c.
- ☑ d.

7) Which of the following is/are true for I/O mapped device interfacing?

     a. Separate address decoder is used to select memory and I/O ports.
     b. Some of the memory address space is occupied by I/O devices.
     c. Same instructions for memory and I/O operations.
     d. All of these,

- ☑ a.
- ☐ b.
- ☐ c.
- ☐ d.

8) Assume that we are executing some program P1, during the execution some interrupts are generated which are listed. Mark the interrupt types which allow the instruction being executed to be completed before handling it.

     a. Timer interrupt
     b. Page fault interrupt
     c. I/O interrupt
     d. All of these.

- ☐ a.
- ☐ b.
- ☐ c.
- ☑ d.

9) **Which of the following statement(s) is/are true for data transfer techniques?**   *1 point*

    a. Interrupt-driven technique transfers data faster than DMA mode of data transfer.

    b. Asynchronous data transfer can be used for high-speed devices.

    c. Interrupt-driven data transfer wastes more CPU time than asynchronous data transfer.

    d. None of these

- [ ] a.
- [ ] b.
- [ ] c.
- [x] d.

10) **Synchronous data transfer mode can be used for keyboard?**   *1 point*

    a. Yes

    b. No

- ( ) a.
- (•) b.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your own answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.